AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions and listings of claims in the above-referenced application:

1. (Currently amended) An integrated circuit (IC) chip comprising:

a square-wave audio signal generator adapted to generate [a] square-wave signal at an audio frequency;

a counter adapted to digitally count from zero to a predetermined number;

a register adapted to hold a volume control value;

a comparator connected to said counter and connected to said register, said comparator adapted to compare a present count from the counter with the volume control value to produce a modulation signal; and

an AND gate connected to said square-wave signal generator and connected to said comparator, said AND gate adapted to combine, in a logical AND operation, the square-wave signal with the modulation signal to generate an output signal that is on, when both the square-wave signal and the modulation signal are on, and off when one or both of the square-wave signal and the modulation signal are off, the output signal from the AND gate coupled directly to a single pin of the IC, the single pin being further coupled to an amplifier subsystem via a filter.

2. (Previously presented) The IC recited in claim 1 wherein said square-wave audio signal generator generates a square-wave audio signal having a frequency within a range from 500 Hz to five KHz.

3. (Original) The IC recited in claim 1 wherein said counter is a 5-bit counter adapted to count from 0 to 31.

4. (Original) The IC recited in claim 1 wherein said counter operates at a counter frequency on the order of MHz.

5. (Original) The IC recited in claim 1 wherein said register is a pulse width register having five bits.

6. (Original) The IC recited in claim 1 wherein the integrated circuit chip is an application specific integrated circuit chip (ASIC).

7. (Currently amended) A method of generating a modulated square-wave audio signal, the method comprising:

generating a square-wave audio signal having a first audio frequency;

repeatedly counting a predetermined range of values generating count signals;

modulating the count signals with a volume control signal resulting in a modulation signal;

modulating the square-wave signal with the modulation signal to generate a modulated square-wave signal that is on when both the square wave signal and the modulation signal are on and off when one or both of the square-wave signal and the modulation signal are off; and

applying the modulated square-wave signal via a single conductor at the interface of an integrated circuit to an amplifier subsystem.

8. (Original) The method recited in claim 7 wherein the first audio frequency is within a range from 500 Hz to five KHz.

9. (Previously presented) The method recited in claim 7 wherein the repeatedly counting step counts from 0 to 31.

10. (Previously presented) The method recited in claim 7 wherein the repeatedly counting step operates at a counter frequency on the order of MHz.

11. (Previously presented) The method recited in claim 7 wherein the volume control signal is set at a value within a range counted by the repeatedly counting step.

12. (Canceled)

13. (Currently amended) An apparatus comprising:

an integrated circuit (IC) ~~chip~~ adapted to generate a modulated square-wave signal;

an amplifier subsystem connected to said IC ~~chip~~ via a single pin associated with each of the IC and the amplifier subsystem, respectively, the amplifier subsystem adapted to filter and amplify the modulated square-wave signal, wherein said IC ~~chip~~ comprises:

a square-wave signal generator adapted to generate a square-wave signal at an audio frequency;

a counter adapted to digitally count from zero to a predetermined number;

a register adapted to hold a volume control value;

a comparator connected to said counter and connected to said register, said comparator adapted to compare a present count from the counter with the volume control value to produce a modulation signal; and

an AND gate connected to said square-wave signal generator and connected to said comparator, said AND gate adapted to combine, in a logical AND operation, the square-wave signal with the modulation signal to generate a modulated output signal that is on, when both the square wave signal and the modulation signal are on, and off when one or both of the square-wave signal and the modulation signal are off.

14. (Previously presented) The apparatus recited in claim 13 wherein said square-wave signal generator generates a square-wave signal having a frequency within a range from 500 Hz to five KHz.

15. (Original) The apparatus recited in claim 13 wherein said counter is a 5-bit counter adapted to count from 0 to 31.

16. (Original) The apparatus recited in claim 13 wherein said counter operates at a counter frequency on the order of MHz.

17. (Original) The apparatus recited in claim 13 wherein said register is a pulse width register having five bits.

18. (Original) The apparatus recited in claim 13 wherein said amplifier subsystem comprises a resistor-capacitor (RC) filter connected to a fixed gain amplifier.